



2P0500

V1. 02

4247 2;



2P0500

2P0500

BIOS



\$E 10h0 1 Q& P1`1 1 1 \$E 001h0 1 Q& P1`1 1 1 1 1









































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8 LSU

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1 AFE/CIS

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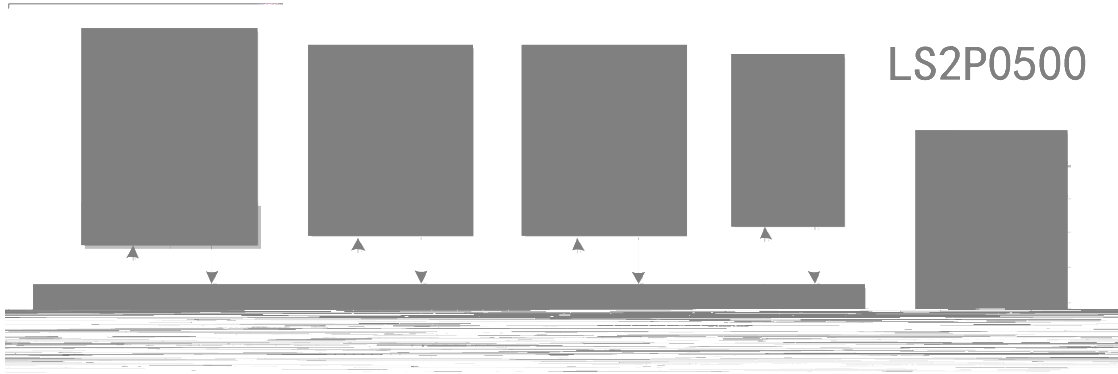
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DFS/DPM

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1.1





-
-

GMAC

-
-
-
-
-
-
-
-

SPI

-
-
-
-
-
-

UART

- 1 UART TXD,RXD,CTS, RTS, DSR,DTR,DCD, RI
- 8 UART /
-
-
- 16
-
-

I²C

-
-
-
-
-
-



-
-
-

- JBIG85

- 8

-

- JPEG

- 1 AFE CIS

DA

- 4 8 DA

PMIO

- 3 PMIO

- 80 IO

PWM

- 32

-

- 40

SDIO

- 2 SDIO

- 1 SDIO (SDIO0 eMMC)

HPET

- 32

- 1

- 2

RTC

-

-



GPIO

- 139 GPIO
-
-

Watchdog

-
-

- 0 70°C()
-

-
-
-
-



2.1

2P0500



2.3

2.4

2.5



2.6

2.7

2.8

2.9





2.15

2.16

2.17

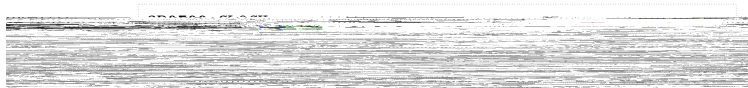


2.18

2.19 Ω



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3.1

sys clock

3-2





SYS PLL

- 1) node_pllclk NODE 500-750MHz
- 2) la132_pllclk LA132 100-400MHz
- 3) soc_pllclk USB GMAC 100-200MHz

- 1) node_pllclk=refclk/div_ref*div_loopc/odiv_node
- 2) la132_pllclk=refclk/div_ref*div_loopc/odiv_la132
- 3) soc_pllclk=refclk/div_ref*div_loopc/odiv_soc

node_pllclk	500-750MHz	PLL	
		refclk/div_ref	20~40MHz PLL
refclk/div_ref*div_loopc	1.2GHz~3.2GHz	2	PLL

PLL divout

PLL

freq_scale

5.4.21

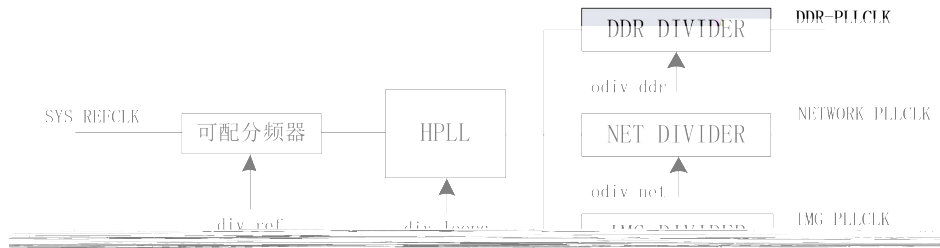
3.2

DDR PLL SYS PLL

- 1) ddr_pllclk 300-400MHz
- 2) network_pllclk NETWORK 200-400MHz
- 3) img_pllclk IMAGE 100-300MHz

PLL divout

PLL



3.3

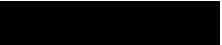
VID PLL	PLL	
1) prvid_pllclk		100-400MHz
2) scvid_pllclk		100-300MHz
	PLL	divout
		PLL

3.4

3 PLL
SYS_CLKSEL[1:0]

3.4.1







4.1

- (
-
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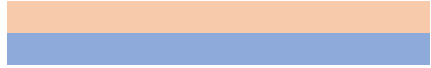
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4.2



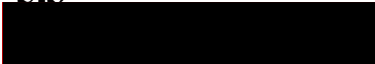
5.1





- (1) -
Confbus(AXI)
BOOT(AXI)
DEVs(APB)
OTG/GMAC(Resume)
- (2) PRT (PR-SRAM/DEVs)
- (3) SCAN (SC-DEVs)

5.3





1. PLL PD 1
2. sel_pll_* soft_set_pll
0
3. PLL PD 0
4. soft_set_pll 1
5. locked_* 1
6. sel_pll_* 1

PLL



$$\text{clock_out} = \text{refclk} / \text{div_ref} * \text{loopc} / \text{divoutN}$$

2P0500 refclk 100MHz refclk / div_ref
 20 ~ 40MHz refclk / div_ref * loopc 1.2GHz ~ 3.2GHz













5. 4. 8

0

5. 4. 9

1

5. 4. 10

GPI 00~15



5. 4. 11

GPI 016-31



5. 4. 12

GPI 032~43



5. 4. 13 USB PHY 0



5. 4. 14 USB PHY 1



5. 4. 15 SYS PLL 0

5. 4. 16 SYSPLL 1



5. 4. 17 DDR PLL 0

5. 4. 18 DDR PLL 1

5. 4. 19 VI D PLL 0





5. 4. 22

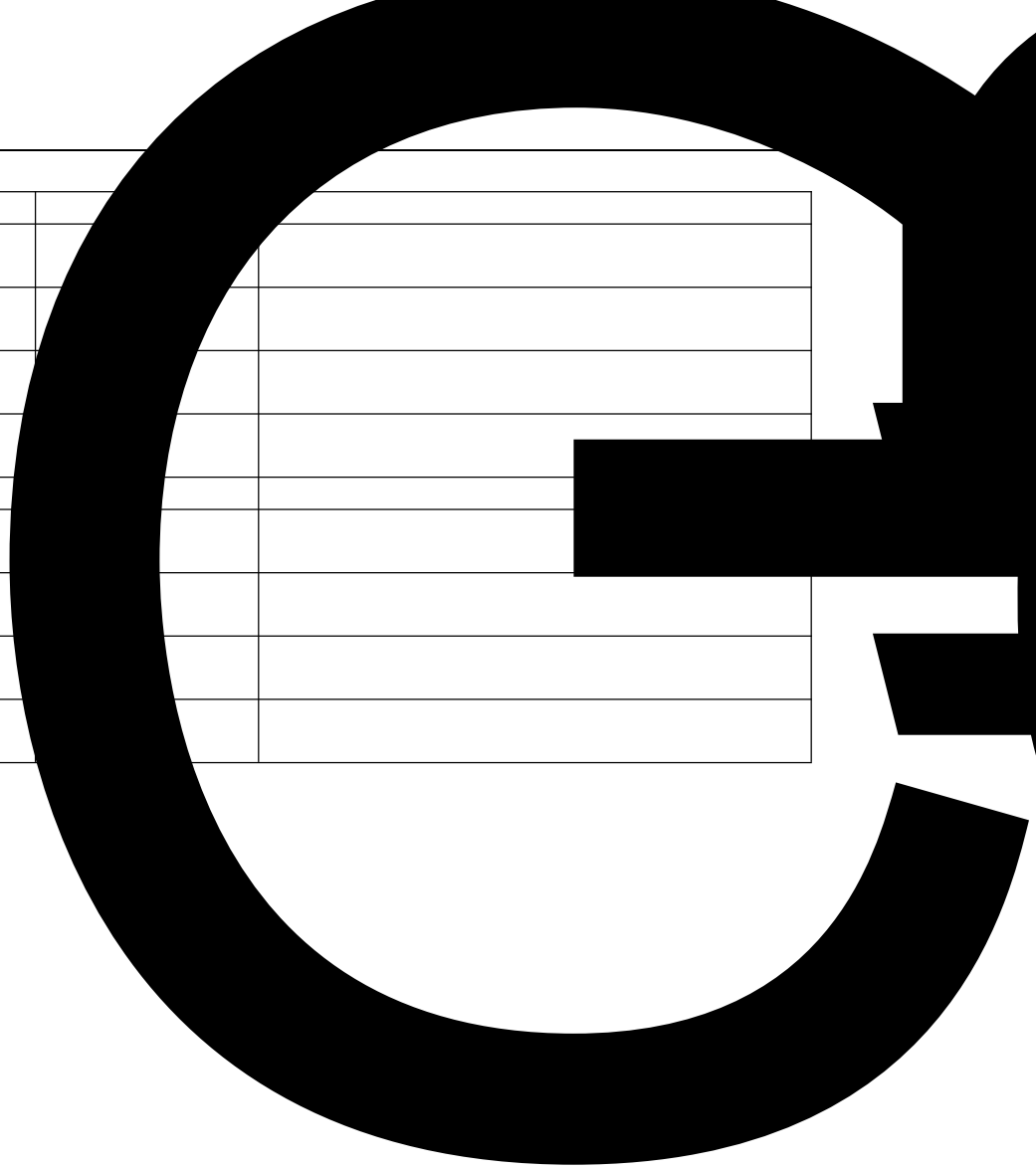
1







5. 4. 26





5. 4. 27

GPI 00-15



5. 4. 30

GPI 048-57

5. 4. 31

0



5. 4. 32

1

5. 4. 33





5. 4. 34

5. 4. 35

DNA

5. 4. 36

0







5. 4. 39

5. 4. 40

0 MAILBOX



5. 4. 45 1 MAI LBOX

5. 4. 46 1 MAI LBOX

5. 4. 47 1 MAI LBOX

5. 4. 48 1 MAI LBOX

5. 4. 49 1 MAI LBOX 0-7



5. 4. 50 2 MAI LBOX

5. 4. 51 2 MAI LBOX

5. 4. 52 2 MAI LBOX

5. 4. 53 2 MAI LBOX



5. 4. 56

5. 4. 57

5. 4. 58

GPI 00-15







5. 4. 63

31:0	SCACHIP_HPT			

5. 4. 64

5. 4. 65 0 MAILBOX

5. 4. 66 0 MAILBOX



5. 4. 67 0 MAILBOX

5. 4. 68 0 MAILBOX

5. 4. 69 0 MAILBOX 0-7

5. 4. 70 1 MAILBOX



5. 4. 71 1 MAI LBOX

5. 4. 72 1 MAI LBOX

5. 4. 73 1 MAI LBOX

5. 4. 74 1 MAI LBOX 0~7



5. 4. 75 2 MAI LBOX

5. 4. 76 2 MAI LBOX

5. 4. 77 2 MAI LBOX

5. 4. 78 2 MAI LBOX



5. 4. 79

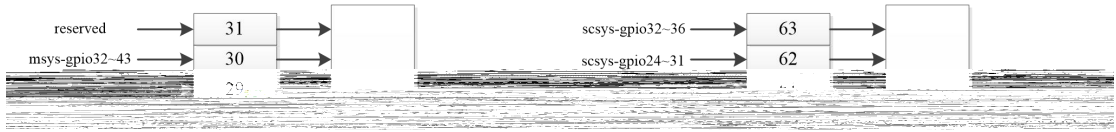
2 MAI LBOX

0-7

5. 4. 80

MAI LBOX

5.5



	5-94	Enable	Intenset	Intenclr	Inten
Intenset		Intenset	1	Intenclr	
Intenclr	1			Inten	
()				Intedge	
1	0	Intpol			0
		1			0
		1			
Intenclr		,			
	Intenset				





	5-97	Enable	INT_IEN	INT_IEN
INT_IEN	1			INT_CLR
INT_CLR	1			
			INT_EDGE	1
0				INT_POL
	0	1		INT_DUAL
INT_POL		0	1	
INT_CLR				











6.1

DDR3

0x0FF0_0000	0x0FFF_FFFF		mc_default_reg = 1 mc_default_reg = 0 mc_disable_reg = 0
			X2 DDR

mc_default_reg mc_disable_reg 0

2P0500 1 CS 1 19

16 3 Bank

DDR3

CS_n 1 RAS_n 16 CAS_n

16 BANK_n 3

CPU

2P0500

1

2

3

4

DCC

5

133-400MHz

6.2



	63:56	55:48	47:40	39:32	31:24	23:16	15:8	7:0
0x000	Dll_value_0(RD)/Dll_adj_cnt/dll_sync_disable/dll_close_disable		Dll_value_ck(RD)		Dll_init_done(RD)		Version(RD)	
0x008	Dll_value_4(RD)		Dll_value_3(RD)					

	63:56	55:48	47:40	39:32	31:24	23:16	15:8	7:0
0x260	Ecc_addr(RD)							
0x268	Ecc_data(RD)							
0x270	Lpbk_ecc_mask(RD)	Prbs_init			Lpbk_error(RD)	Prbs_23	Lpbk_start	Lpbk_en
0x278	Lpbk_ecc(RD)		Lpbk_data_mask(RD)		Lpbk_correct(RD)		Lpbk_counter(RD)	
0x280	Lpbk_data_r(RD)							
0x288	Lpbk_data_f(RD)							
0x290	Axi0_bandwidth_w				Axi0_bandwidth_r			
0x298	Axi0_latency_w				Axi0_latency_r			
0x2A0	Axi1_bandwidth_w				Axi1_bandwidth_r			
0x2A8	Axi1_latency_w				Axi1_latency_r			
0x2B0	Axi2_bandwidth_w				Axi2_bandwidth_r			
0x2B8	Axi2_latency_w				Axi2_latency_r			
0x2C0	Axi3_bandwidth_w				Axi3_bandwidth_r			
0x2C8	Axi3_latency_w				Axi3_latency_r			
0x2D0	Axi4_bandwidth_w				Axi4_bandwidth_r			
0x2D8	Axi4_latency_w				Axi4_latency_r			
0x2E0	Cmdq0_bandwidth_w				Cmdq0_bandwidth_r			
0x2E8	Cmdq0_latency_w				Cmdq0_latency_r			
0x2F0	Cmdq1_bandwidth_w				Cmdq1_bandwidth_r			
0x2F8	Cmdq1_latency_w				Cmdq1_latency_r			
0x300	Cmdq2_bandwidth_w				Cmdq2_bandwidth_r			
0x308	Cmdq2_latency_w				Cmdq2_latency_r			
0x310	Cmdq3_bandwidth_w				Cmdq3_bandwidth_r			
0x318	Cmdq3_latency_w				Cmdq3_latency_r			
0x320	tRESYNC_length	tRESYNC_shift	tRESYNC_max	tRESYNC_min	Pre_predict		tXS	tREF_low
0x328								tRESYNC_delay
0x330	Stat_en	Rdbuffer_max	Retry	Wr_pkg_num	Rwq_rb	Stb_en	Addr_new	tRDQidle
0x338				Rd_fifo_depth	Retry_cnt			
0x340	tREFretention					Ref_num	tREF_IDLE	Ref_sch_en
0x348								
0x350	Lpbk_data_en							
0x358						Lpbk_ecc_mask_en	Lpbk_ecc_en	Lpbk_data_mask_en
0x360			Int_ecc_cnt_fatal	Int_ecc_cnt_error	Ecc_cnt_cs_3	Ecc_cnt_cs_2	Ecc_cnt_cs_1	Ecc_cnt_cs_0
0x368								
0x370	Prior_age3		Prior_age2		Prior_age1		Prior_age_0	
0x378							No_dead_inorder	Row_hit_place
0x380	Zq_cnt_1				Zq_cnt_0			
0x388	Zq_cnt_3				Zq_cnt_2			
0x390								Nc16_map
0x398								



7.1

7.2





8.1

2P0500 USB

- USB Rev 1.1 USB Rev 2.0
- OHCI Rev 1.0 EHCI Rev 1.0
- LS Low Speed FS Full Speed HS High Speed USB
- USB2.0 LS FS HS

USB

EHCI

OHCI

EHCI

OHCI

EHCI

8.2



9.1

2P0500 OTG :

- HNP SRP
- DMA OTG
- device 480Mbps
- host 480Mbps
- device 10 endpoint endpoint0
- device 4 IN
- host 12 channel channel
- host periodic OUT

9.2

AHB slave OTG CSRs

32 32

host device

Core Global Power and Clock Gating FIFO

Data FIFO Access Host Port OTG host

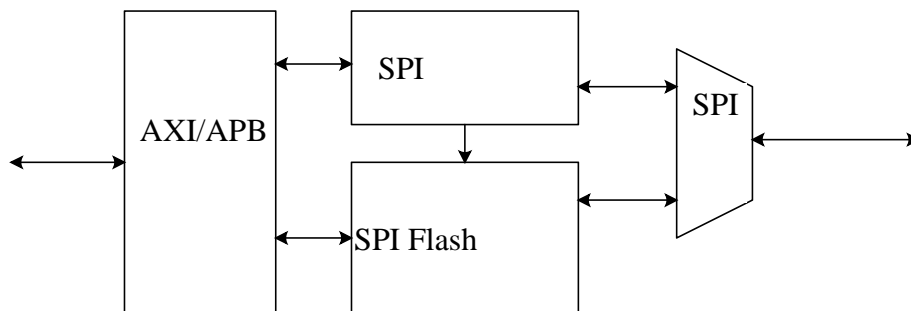
device

Mode Mismatch , Core Interrupt Register .

OTG

10.1

SPI
SPI 2.19
GPIO





10.2

(SPCR)

7				
6				
5				
4				
3				
2				
1:0				

(SPSR)

7				
6				
5:4				
3				
2				
1				
0				

(TxFIFO/RxFIFO)

(SPER)



7:6				
5:3				
2				
1:0				

(SFC_PARAM)

7:4				
3				
2				
1				
0				

(SFC_SOFTCS)

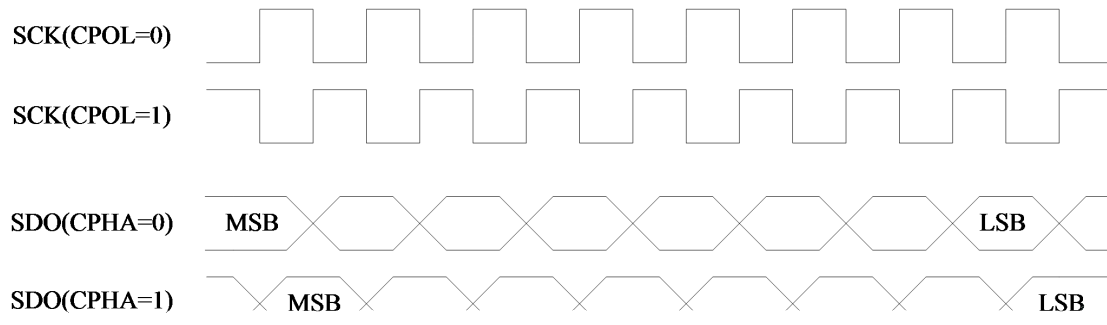
7:4				
3:0				

(SFC_TIMING)

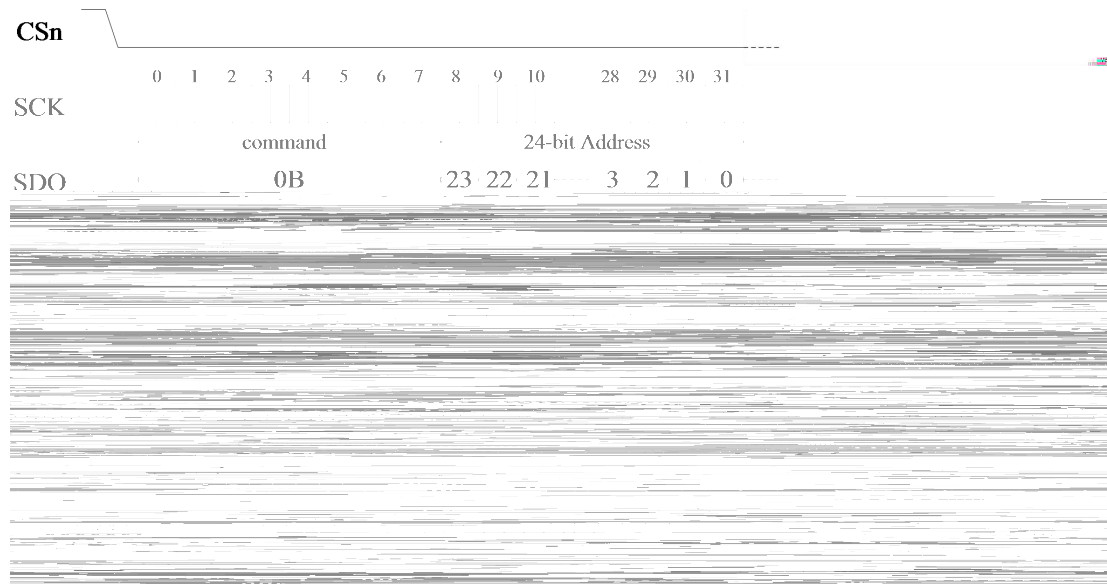
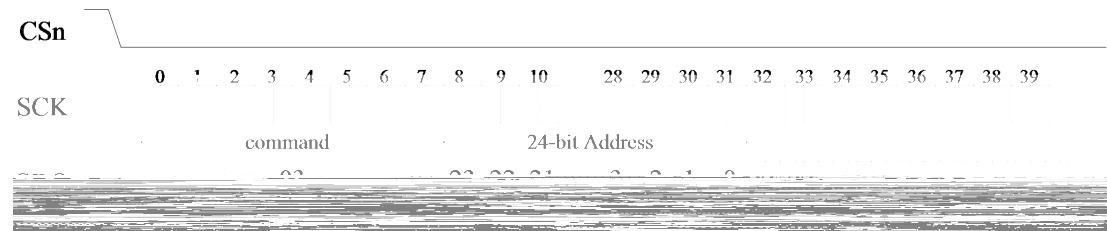
7:3				
2				
1:0				

10.3

SPI

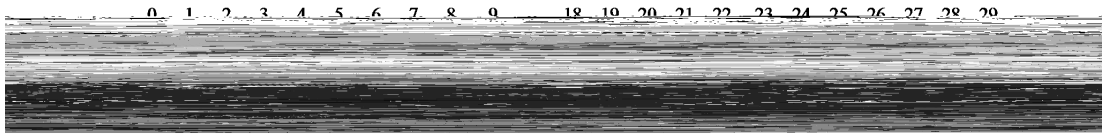


SPI Flash





CSn



10.4

SPI

1.

-
-
-
-

2.

/

-
-

3.

-
-
-
-

SPI Flash

1.



-
-

2.

SPI Flash SPI

1. **SPI Flash**



11.1

11.2

1(CR1)



2(CR2)





4(CR4)



2(SR2)



1(CFG1)

2(CFG2)





CRC 1(CRC1)

CRC 2(CRC2)

(DR)



DMA

n(CCRn)

31 14				
13 12				
11 10				
9 8				
7				
6				
5				
4				
3				
2				
1				
0				



DMA (CNDTRn)

31 16				
15 0				

DMA (CMARn)

31 16				
15 0				



12.1



12.3

I2C

PRERIo

PRERhi



prescale APB PCLK clock_a SCL
clock_s

CTR

/

TXD/RXD



CR

I2C

ack

ack

0 bit 3 1

SR



BLTOP

SADDR



13.1

/

4

13.2



14.1

14.2





16.1

16.2

16.2.1

CMD

0x00

32'h0

31			
31 17			
16			
15 5			
4			



3			
2 1			
0			

16.2.2

STS

0x04

32'h0

31 1			
0			

Q_TABLE_ADDR

0x08

32'h0

31 4			
3 0			

16.2.4

BLOCK_OF_IMAGE

0x0c

32'h0

31 0			
------	--	--	--



31 4			
3 0			

16.2.6

JPEG_OUT_ADDR

0x14

32'h0

31 4			
3 0			

16.2.7

ENCODING_BYTE

0x18

32'h0



31 0



16.3

JPEG



17.1



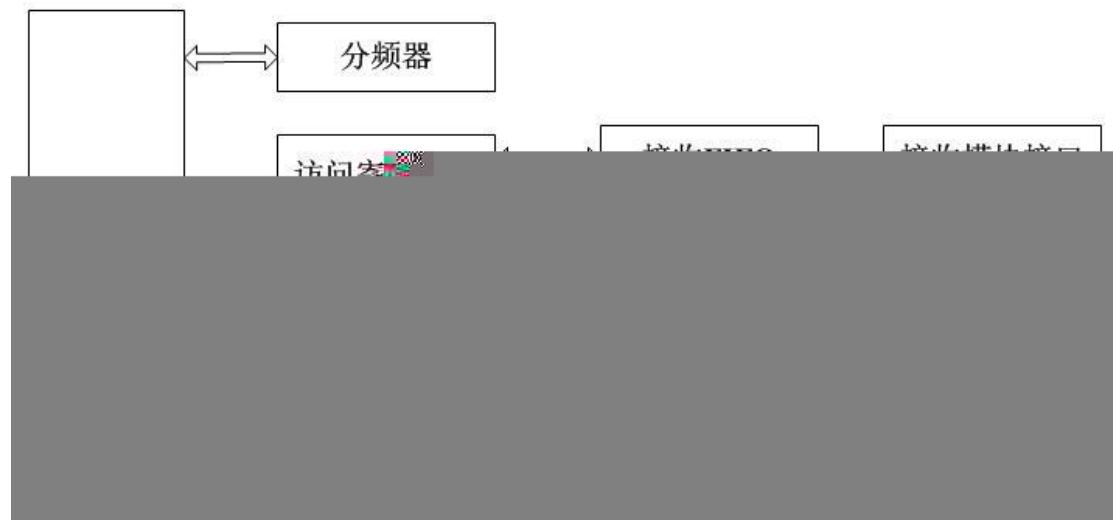




17.3

18.1

18.2





18.3

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-
-
-
-

UART

0x00	DAT/DL_L	/	8
0x01	IER/DL_H	/	8
0x02	IIR		
0x02	FCR/DL_D	FIFO	/
0x03	LCR		
0x04	MCR	Modem	
0x05	LSR		
0x06	MSR	Modem	

UART

UART

2.20

GPIO

DAT



IER

IIR





HYM





19

19.1 DES

19.1.1 DES

DES	32	APB	DES/TDEA	/	
APB	DMA	DES	OpenCore	DES3	/
	/		16	DES	/
48		TDEA	/	DES	
2	APB		DES	/	DES
		2	4	64bit	FIFO
DES			Command	3	64bit
	Key0	Key1	Key2	Key1	Key2
				TDEA	
				Command[1]	
	Data_low	Data_high	FIFO	DES	FIFO
	/			FIFO	APB
Command[4]			Command[4]	0	APB
	Data_low	Data_high	FIFO		

19.1.2 DES

DES	PCI	(dev29,func1)	DES
	6		

19.1.3 DES

DES

0x0	Key0_low	DES	32	/TDEA	0 32
0x4	Key0_high	DES	32	/TDEA	0 32
0x8	Key1_low	TDEA	1	32	
0xc	Key1_high	TDEA	1	32	
0x10	Key2_low	TDEA	2	32	
0x14	Key2_high	TDEA	2	32	



0x18	Data_low	DMA	Command[2] = 1'b0	/	32
				/	32
		DMA	Command[2] = 1'b1	Data_low	Data_high
				/	32
					32
0x1c	Data_high	DMA	Command[2] = 1'b0	/	32
				/	32
		DMA	Command[2] = 1'b1	Data_low	Data_high
				/	32
					32
0x20	Command				
0x24	Rev				
0x28					
0x2c					

Comand

0	0	des3	RW	0	DES
				1	TDEA
1	0	decrypt	RW	0	
				1	
2	0	dma_start	RW	1	DMA
					0
					DMA
					1
3	0	dma_done	RWIC	DMA	1
					1
4	1	dout_empty	RO	0	FIFO
				1	FIFO
5	0	din_full	RO	0	FIFO
				1	FIFO
7:6	0	Rev	RO		
31:8	0	dma_count	RW		DMA / 64

19.2 AES

19.2.1 AES

AES 32 APB 128-bit KEY 192-bit KEY 256-bit KEY



AES / APB DMA DMA
 CTR / AES 3 KEY
 / 11 128-bit KEY AES / 13
 192-bit KEY AES / 15 256-bit KEY AES /
 / AES 2 APB
 AES / AES KEY
 APB 2 4 128bit FIFO /
 AES Command AES
 8 32bit Key0
 Key1 Key2 key3 key4 key5 key6 key7 Key4 Key5 192-bit KEY 256-bit
 KEY Key6 Key7 256-bit KEY
 Command[1] 4 32 Data0 Data1 Data2
 Data3 FIFO AES FIFO /
 FIFO APB Command[4]
 Command[4] 0 APB Data0 Data1 Data2 Data3
 FIFO

19.2.2 AES

AES PCI (dev29,func0) AES
 6

19.2.3 AES

AES





Comand





EMMC_PRE			
emmc_clk_rev_en	31	0x1	
Reserved	30:8	0x0	-
emmc_pre	7:0	0x1	eMMC =PCLK/

		/ (R/W)			
EMMC_CMD_ARG	0x08	R/W	eMMC		0x0

EMMC_CMD_ARG			
sdi_cmd_arg	31:0	0x0	

		/ (R/W)			
EMMC_CMD_CON	0x0c	R/W	eMMC		0x0

EMMC_CMD_CON			
Reserved	31:18	0x0	
func_num_abort	17:15	0x0	eMMC auto_stop_en 0
emmc_en	14	0x0	eMMC 1 CMD52 0 CMD12 auto_stop_en 0
check_on	13	0x0	CRC 1
Auto_stop_en	12	0x0	1
Reserved	11	0x0	-
long_rsp	10	0x0	136 1
Wait_rsp	9	0x0	1
CMST	8	0x0	1
cmd_index	7:0	0x0	2 8



		/ (R/W)		
EMMC_CMD_STA	0x10	RO	eMMC	0x0

EMMC_CMD_STA			
Reserved	31:13	0x0	-
cmd_sent_fin	14	0x0	1
auto_stop	13	0x0	1 0
rsp_crc_err	12	0x0	CRC CRC 1 CRC 0
cmd_end	11	0x0	1 0
cmd_tout	10	0x0	64 R1b 1 0
rsp_fin	9	0x0	1 0
cmd_on	8	0x0	1 0
rsp_index	7:0	0x0	2 8

		/ (R/W)		
EMMC_RSP0	0x14	RO	eMMC	0 0x0

EMMC_RESP0			
sdi_resp0	31:0	0x0	[31:0] [127:96] sdi_cmd_con[10]

		/ (R/W)		
EMMC_RSP1	0x18	RO	eMMC	1 0x0

EMMC_RESP1			
sdi_resp1	31:0	0x0	[95:64] sdi_cmd_con[10]



		/ (R/W)		
EMMC_RSP2	0x1c	RO	eMMC 2	0x0

EMMC_RESP2				
sdi_resp2	31:0	0x0	[63:32] sdi_cmd_con[10]	

		/ (R/W)		
EMMC_RSP3	0x20	RO	eMMC 3	0x0

EMMC_RESP3				
sdi_resp3	31:0	0x0	[31:0] sdi_cmd_con[10]	

		/ (R/W)		
EMMC_DTIMER	0x24	R/W	eMMC	0x0

EMMC_DTIMER				
Reserved	31:24	0x0		
sdi_dtimer	23:0	0x0		

		/ (R/W)		
EMMC_BSIZE	0x28	R/W	EMMC	0x0

EMMC_BSIZE				
Reserved	31:12	0x0		
sdi_bsize	11:0	0x0	0~4095	

		/ (R/W)		
EMMC_DAT_CON	0x2c	R/W	eMMC	0x0



EMMC_DAT_CON			
Reserved	31:21	0x0	-
wide_mode_8b	26	0x0	wide_mode_8b 1 wide_mode 0 eMMC
resume_rw	20	0x0	eMMC 1 eMMC 0
IO_resume	19	0x0	eMMC EMMC 1 IO_suspend 0 EMMC
IO_suspend	18	0x0	eMMC 1 CMD52 eMMC 0.
RwaitReq	17	0x0	1 DAT2 eMMC 0
wide_mode	16	0x0	1 4 0
DMA_en	15	0x0	DMA 1 DMA 0 DMA
DTST	14	0x0	1
Reserved	13:12	0x0	-
Blk_num	11:0	0x0	

		/ (R/W)		
EMMC_DAT_CNT	0x30	R/W	eMMC	0x0

EMMC_DAT_CNT			
Reserved	31:24	0x0	
blk_num_cnt	23:12	0x0	
blk_cnt	11:0	0x0	

		/ (R/W)		
EMMC_DAT_STA	0x34	RO	eMMC	0x0



EMMC_DAT_STA			
Reserved	31:17	0x0	-
suspend_on	16	0x0	1
rst_suspend	15	0x0	1 FIFO DMA eMMC
R1b_tout	14	0x0	1 R1b
data_start	13	0x0	1
R1b_fin	12	0x0	busy busy 0 busy 1
auto_stop	11	0x0	1
Reserved	10	0x0	-
r_wait_req	9	0x0	EMMC
EMMC_int	8	0x0	eMMC 1
crc_sta	7	0x0	CRC
dat_crc	6	0x0	CRC
dat_tout	5	0x0	1
dat_fin	4	0x0	1
busy_fin	3	0x0	1
prog_err	2	0x0	1
tx_dat_on	1	0x0	Tx 1 0
rx_dat_on	0	0x0	Rx 1 0

EMMC_FIFO_STA	0x38	/ (R/W)	eMMC FIFO	0x0
		RO		

EMMC_FIFO_STA			
Reserved	31:12	0x0	-
tx_full	11	0x0	Tx FIFO
tx_empty	10	0x0	Tx FIFO
Reserved	9	0x0	-
rx_full	8	0x0	Rx FIFO
rx_empty	7	0x0	Rx FIFO
Reserved	6:0	0x0	-

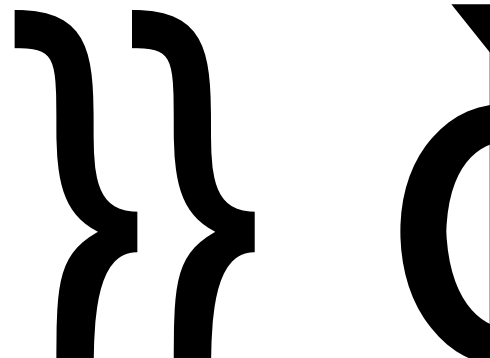
EMMC_INT_MASK	0x3c	/ (R/W)	eMMC	0x0
		R/W		



EMMC_INT_MASK			
Reserved	31:10	0x0	-
R1b_fin_int	9	0x0	busy 1
rsp_crc_int	8	0x0	CRC 1
cmd_tout_int	7	0x0	1
cmd_fin_int	6	0x0	
EMMC_int	5	0x0	eMMC 1
prog_err_int	4	0x0	1
crc_sta_int	3	0x0	CRC 1
dat_crc_int	2	0x0	CRC 1
dat_tout_int	1	0x0	1
dat_fin_int	0	0x0	

EMMC_DAT	0x40	/ (R/W)	eMMC	0x0
		RO		

EMMC_DAT			
emmc_dat	31:0	0x0	eMMC DMA





dll_master_val	0xf0	/ (R/W) R	DLL master	0x0
----------------	------	--------------	------------	-----



sdio_emmc_sel	0xfc	/ (R/W)	
---------------	------	---------	--



DMA_SADDR

DMA_DADDR

DMA_LENGTH

step length step 1
DMA

DMA_STEP_LENGTH

step



DMA_STEP_TIMES

DMA

1

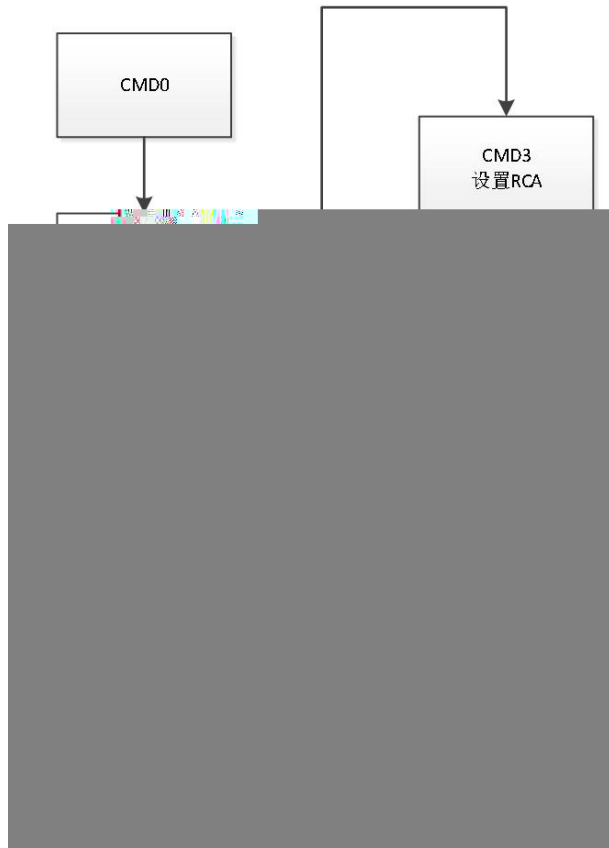
DMA_CMD







20.5.2 eMMC





20. 5. 3 DDR



21 SDIO

21.1

- 2P0500 SDIO/eMMC SD Memory SDIO
- SD Memory SDIO
- 8 32 / FIFO
 - 256 SD
 - 8 = /(p+1)
 - DMA
 - DMA
 - 1 /4 SD

21.2

SDIO

SDIO

SDIO 2.19 SDIO

GPIO

21.3

SDIO :

		/ (R/W)		
SDI_CON	0x00	R/W	SDIO	0x0

SDI_CON			
Reserved	31:9	0x0	-
soft_rst	8	0x0	
Reserved	7:1	0x0	-
enclk	0	0x0	SD



		/ (R/W)		
SDI_PRE	0x04	R/W	SDIO	0x1

SDI_PRE				
sdio_clk_rev_en	31	0x1	SDR 1 0 sdio DDR	sdio sdio 1
Reserved	30:8	0x0		
Sdi_pre	7:0	0x1	SDIO	=PCLK/

		/ (R/W)		
SDI_CMD_ARG	0x08	R/W	SDIO	0x0

SDI_CMD_ARG				
sdi_cmd_arg	31:0	0x0		

		/ (R/W)		
SDI_CMD_CON	0x0c	R/W	SDIO	0x0

SDI_CMD_CON				
Reserved	31:18	0x0	-	
func_num_abort	17:15	0x0	SDIO	
sdio_en	14	0x0		auto_stop_en 0



		/ (R/W)		
SDI_CMD_STA	0x10	RO	SDIO	0x0

SDI_CMD_STA			
Reserved	31:13	0x0	-
cmd_sent_fin	14	0x0	1
auto_stop	13	0x0	1 0
rsp_crc_err	12	0x0	CRC CRC 1 CRC 0
cmd_end	11	0x0	1 0
cmd_tout	10	0x0	64 R1b 1 0
rsp_fin	9	0x0	1 0
cmd_on	8	0x0	1 0
rsp_index	7:0	0x0	2 8

		/ (R/W)		
SDI_RSP0	0x14	RO	SDIO	0 0x0

SDI_RESP0			
sdi_resp0	31:0	0x0	[31:0] [127:96] sdi_cmd_con[10]

		/ (R/W)		
SDI_RSP1	0x18	RO	SDIO	1 0x0

SDI_RESP1			
sdi_resp1	31:0	0x0	[95:64] sdi_cmd_con[10]



		/ (R/W)		
SDI_RSP2	0x1c	RO	SDIO 2	0x0

SDI_RESP2			
sdi_resp2	31:0	0x0	[63:32] sdi_cmd_con[10]

		/ (R/W)		
SDI_RSP3	0x20	RO	SDIO 3	0x0

SDI_RESP3			
sdi_resp3	31:0	0x0	[31:0] sdi_cmd_con[10]

		/ (R/W)		
SDI_DTIMER	0x24	R/W	SDIO	0x0

SDI_DTIMER			
Reserved	31:24	0x0	-
sdi_dtimer	23:0	0x0	

		/ (R/W)		
SDI_BSIZE	0x28	R/W	SDIO	0x0

SDI_BSIZE			
Reserved	31:12	0x0	
sdi_bsize	11:0	0x0	0~4095

		/ (R/W)		
SDI_DAT_CON	0x2c	R/W	SDIO	0x0



SDI_DAT_CON			
Reserved	31:21	0x0	-
resume_rw	20	0x0	SDIO 1 SDIO 0
IO_resume	19	0x0	SDIO SDIO 1 IO_suspend 0 SDIO
IO_suspend	18	0x0	SDIO 1 CMD52 SDIO 0.
RwaitReq	17	0x0	1 DAT2 SDIO 0
wide_mode	16	0x0	1 4 0
DMA_en	15	0x0	DMA 1 DMA 0 DMA
DTST	14	0x0	1
Reserved	13:12	0x0	-
Blk_num	11:0	0x0	

		/ (R/W)		
SDI_DAT_CNT	0x30	R/W	SDIO	0x0

SDI_DAT_CNT			
Reserved	31:24	0x0	-
blk_num_cnt	23:12	0x0	
blk_cnt	11:0	0x0	

		/ (R/W)		
SDI_DAT_STA	0x34	RO	SDIO	0x0

SDI_DAT_STA			
Reserved	31:17	0x0	-
suspend_on	16	0x0	1



SDI_DAT_STA			
rst_suspend	15	0x0	1
			FIFO DMA
R1b_tout	14	0x0	1
data_start	13	0x0	1
R1b_fin	12	0x0	busy
			0 busy
auto_stop	11	0x0	1
Reserved	10	0x0	-
r_wait_req	9	0x0	
SDIO_int	8	0x0	SDIO 1
crc_sta	7	0x0	CRC
dat_crc	6	0x0	CRC
dat_tout	5	0x0	1
dat_fin	4	0x0	1
bus i			



SDI_INT_MASK

Reserved	31:10	0x0			
R1b_fin_int	9	0x0	busy	1	
rsp_crc_int	8	0x0	CRC	1	
cmd_tout_int	7	0x0		1	
cmd_fin_int	6	0x0			
SDIO_int	5	0x0	SDIO	1	
prog_err_int	4	0x0	SD	1	
crc_sta_int	3	0x0		CRC	1
dat_crc_int	2	0x0	CRC	1	
dat_tout_int	1	0x0		1	
dat_fin_int	0	0x0			

param_delay				
	31:16	0x0		
clk_rd_delay	15:8	0x0	DDR	clk_pad_delay
clk_pad_delay	7:0	0x0		50MHz 20ns
				50 50*100ps

		/ (R/W)	
sdio_emmc_sel	0xfc	R/W	0x0

sdio_emmc_sel			
reserved	31:4	0x0	-
bus_sel	1	0x0	SDIO EMMC 0 SDIO 1 EMMC EMMC EMMC
data_mode	0	0x0	0 SDR 1 DDR

21.4

21.4.1 SD Memory

SD Memory

1. sdi_con
2. sdi_pre



M

➤ sdi_rsp

CMD0 CMD8 ACMD41(CMD55 CMD41) 02 CMD3

CMD7 ACMD6 4bit

5. Bsize Dtimer

6. DMA dat_con DMA SDIO

0x800 DMA 0x400 DMA eMMC DMA

7. sdi_int_msk

8.

21. 4. 2 SDIO

SDIO SD memory

1. sdi_con

2. sdi_pre

3.

4. sdi_int_en

5.

➤ cmd_arg

➤ cmd_con

➤ sdi_int_msk

➤ sdi_rsp

CCCR

CMD52 CMD5 CMD3(RCA) CMD7 RCA

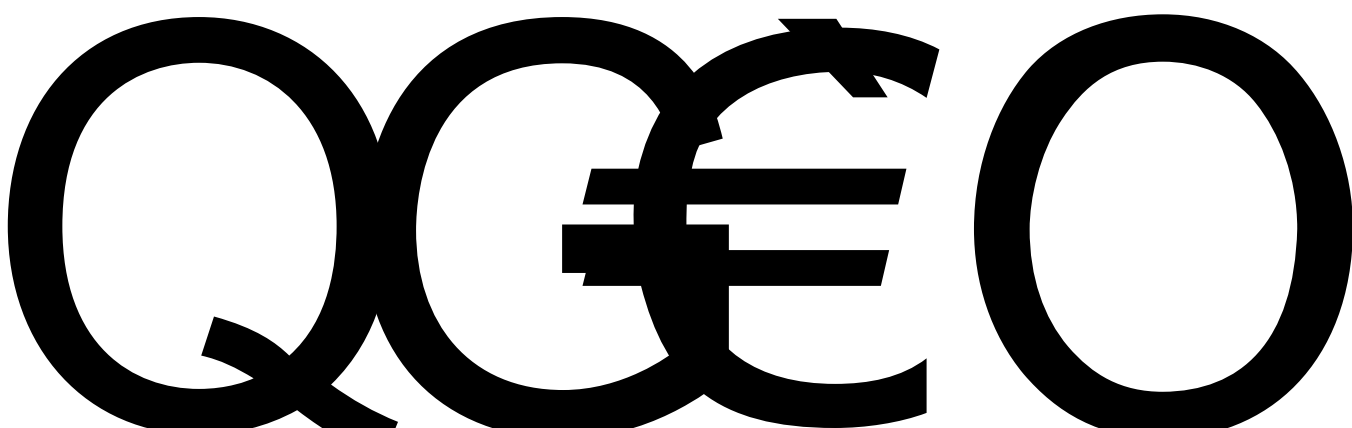
CMD52 4bit CMD52 CMD52

IO Bsize Dtimer

6. DMA dat_con DMA

DMA dat_con

7.





11.

DAT2

SDIO

12.

2

3

1

2



5	INTE	R/W	0	1 full_pulse 1 0
6	INT	R/W	0	1 ,0 1
7	RST	R/W	0	Low_level full_pluse 1 buffer 0
8	CAPTE	R/W	0	1 0
9	INVERT	R/W	0	1 0
10	DZONE	R/W	0	1 0

22.4

22.4.1

Low_buffer Full_buffer
 low_level full_pulse Low_buffer Full_buffer
 low_level
 1 full_pulse full_pulse 1
 low_level full_pulse Low_buffer Full_buffer
 full_pulse
 1
 50 90 low_buffer
 90 full_buffer (50+90)=140
 EN 0 EN 1
 EN
 0 low_buffer 0 full_buffer
 1 Low_buffer full_buffer

CTRL



22.4.2

PWM		CTRL		
Low_level	full_pulse	Low_level	full_pulse	
Low_level	low_buffer			
full_pulse	full_buffer	Low_level	full_pulse	1
	50	90	low_buffer	
90	full_buffer	(50+90)=140		
		32		
	low_buffer	full_buffer		
	0xFFFF_FFF9	INT	1	

22.4.3

PWM

PWM_0 PWM_1 PWM_2 PWM_3



23 HPET

23.1

2P0500

4 HPET

HPET High Precision Event Timer,

up-counter

APB

match

match

HPET

main count

comparator

32



S3 S4 S5

23.3.1 General Capabilities and ID Register

23.3.2 General Configuration Register



23.3.3 General Interrupt Status Register

23.3.4 Main Counter Value Register

23.3.5 Timer N Configuration and Capabilities Register



23.3.6 Timer N Comparator Value Register

		<ul style="list-style-type: none">◆◆◆	

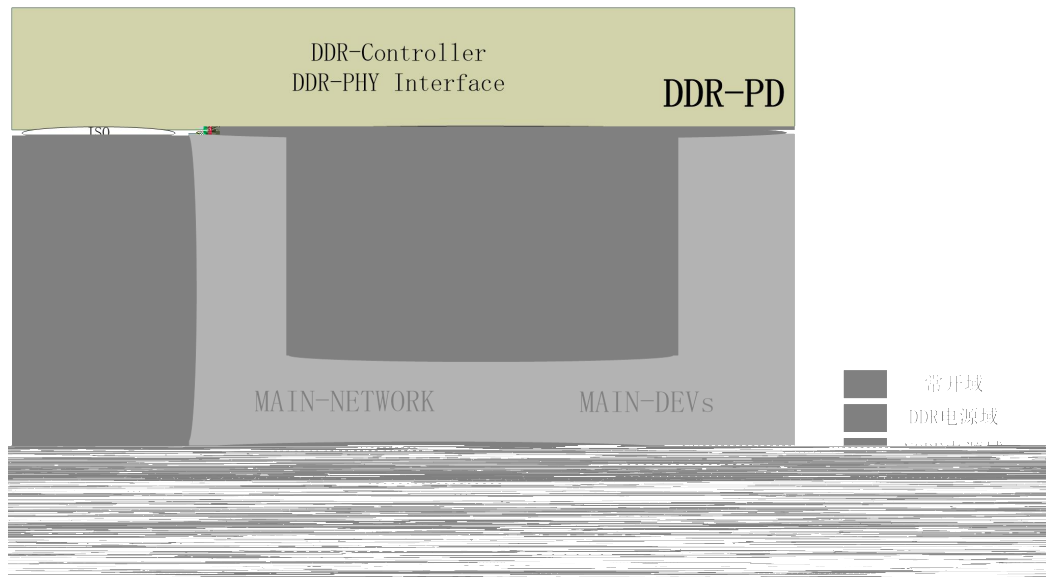


25.1

-
-
-
-
-

25.2

LS2P05xx			
1	(Always-On)		PRINT-LA132 PRT-SRAM PRT-DEVs(UART I2C GPIO DA PWM PM0IO SPI HPET PRINTer)
			OTG GMAC0
2	NODE	LA364 Scache IODMA LIXBAR	
3	DDR	DDR3-Controller DDR3-PHY	
4	IMAGE	JBIG JPEG	
5	SCAN		SCAN-LA132 SCA-DEVs(UART GPIO PM1IO SPI HPET SCANNer)
			NETWORK
6	SYS+NETWORK		BOOT(SPI0+CONFBUS) GMAC1 USB1/2 UART I2C GPIO SPI HPET PM2IO PWM SDIO EMMC ENCRYPT



	DFS			PHY	
NODE (LA364+SCACHE)			-	-	LA132 NODE
PRT-LA132			-	-	
SCA-LA132				-	
DDR	-				DDR PHY
IMAGE	-			-	
	-		-	-	
	-			-	
	-			-	
GMAC0	-		-	-	GMAC0
GMAC1	-			-	
OTG	-		-	-	OTG
USB1/2	-				USB PHY
	-			-	

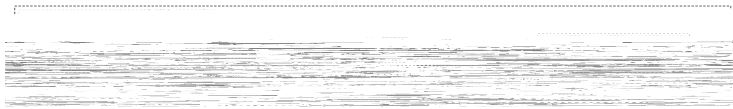


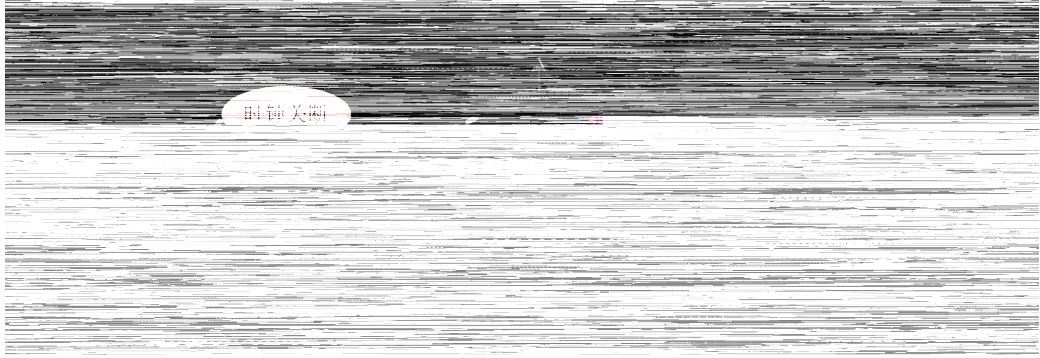
25. 2. 1 DFS





25. 2. 2 DPM

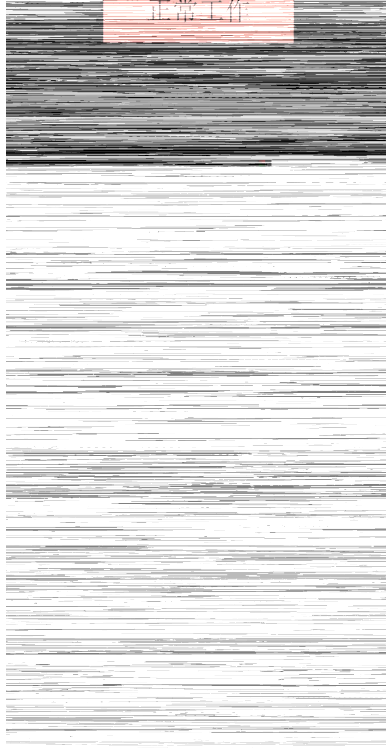




25. 2. 3



正常工作







25.3.1.6 WAIT_TIME1 : Wait Time1 Register

WAIT_TIME1		
Bit	Field Name	Value
7		
6		
5		
4		
3		
2		
1		
0		

25.3.1.7 WAIT_TIME2 : Wait Time2 Register

WAIT_TIME2		
Bit	Field Name	Value
7		
6		
5		
4		
3		
2		
1		
0		

25.3.1.8 WAIT_TIME3 : Wait Time3 Register

WAIT_TIME3		
Bit	Field Name	Value
7		
6		
5		
4		
3		
2		
1		
0		

25.3.1.9 CG_CFG : Clkgate Config Register

CG_CFG		
Bit	Field Name	Value
7		
6		
5		
4		
3		
2		
1		
0		





25. 3. 3 WDT

WDT		

25.3.3.1 WD_EN : Watch Dog Enable Register





25.3.3.3 WD_Timer : Watch Dog Timer Register

25.3.3.4 PLTRST_SET : Planrst Set Register



26. 2. 3 SYS_TOYWRI TE1

TOY

32



26.2.8 SYS_RTCWRITE

RTC
[31 0]
0x64
0x00000000

26.2.9 SYS_RTCREAD

RTC
[31 0]
0x68
0x00000000

26.2.10 SYS_RTCMATCH0/1/2

RTC 0/1/2
[31 0]
0x6C/70/74
0x00000000



27.1

27.2





27.3

GPIO

GPIO

GPIO

GPIO

GPIO

GPIO

GPIO

GPIO



27.4

27.4.1 GPIO

27.4.2 GPIO

27.4.3 GPIO



27. 4. 4 GPI O

27. 4. 5 GPI O



27. 4. 6 GPI O

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27. 4. 7 GPI O



27.4.8 GPIO

27.4.9 GPIO